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CLAIMS

1. A method of fabricating a superconductor integrated circuit from a trilayer comprised of a counter electrode layer, a tunnel barrier layer and a base electrode layer, the method comprising:

etching the counter electrode layer for forming a tunnel junction region and an exposed portion of the tunnel barrier layer, wherein the tunnel junction region is comprised of an unetched portion of the counter electrode layer, an unexposed portion of the tunnel barrier layer and a portion of the base electrode layer;

anodizing the exposed portion of the tunnel barrier layer and sidewall portions of the tunnel junction region for forming an anodized tunnel barrier, an anodized tunnel junction region and a junction contact; and

etching the anodized tunnel barrier for forming an anodization ring surrounding the tunnel junction region.

2. The method of claim 1, wherein:

the etching of the counter electrode layer for forming a tunnel junction region and an exposed portion of the tunnel barrier layer further comprises etching the counter electrode layer over a first junction mask;

the anodizing of the exposed portion of the tunnel barrier layer and sidewall portions of the tunnel junction region further comprises anodizing the exposed portion of the tunnel barrier layer and sidewall portions of the tunnel junction region over the first junction mask; and

the etching of the anodized tunnel barrier for forming an anodization ring surrounding the tunnel junction region further comprises etching the anodized tunnel barrier over a second junction mask.

3. The method of claim 2, further comprising:

anodizing a portion of the base electrode for forming an anodized portion of the base electrode over the first junction mask; and

etching the anodized portion of the base electrode over the second junction mask for forming the anodization ring to include an unetched portion of the anodized portion of the base electrode.

4. The method of claim 3, further comprising:

etching a portion of the base electrode to form an electrode isolation region for device isolation;

depositing an oxide layer over the base electrode, the electrode isolation region and the anodization ring for forming a dielectric layer; and

etching the dielectric layer over a third contact mask for forming a base electrode via and an outside contact via, wherein the anodized tunnel barrier functions as an etch stop during the etching of the dielectric layer.

5. The method of claim 4, wherein the etching of the dielectric layer over a third contact mask for forming a base electrode via and an outside contact via

further comprises forming the outside contact via to have a diameter that is equal to or greater than a diameter of the junction contact.

6. The method of claim 4, further comprising depositing a wire layer over the dielectric layer and the anodization ring for defining a contact wire coupled to the outside contact via and a base electrode wire coupled to the base electrode via.

7. The method of claim 4, wherein the etching of a portion of the base electrode to form an electrode isolation region further comprises forming the electrode isolation region to be disposed approximately 0.75 μm in horizontal distance from the junction contact.

8. The method of claim 3, wherein:

the etching of the anodized tunnel barrier over a second junction mask further comprises etching the anodized tunnel barrier with a CHF3 or chlorine based reactive ion etch; and

the etching of the anodized portion of the base electrode over the second junction mask further comprises etching the anodized portion of the base electrode with another CHF3 based reactive ion etch subsequent to the etching of the anodized tunnel barrier.

9. The method of claim 3, wherein:

the etching of the anodized tunnel barrier over a second junction mask further comprises wet etching the anodized tunnel barrier in an HF chemical mixture; and

the etching of the anodized portion of the base electrode over the second junction mask further comprises wet etching the anodized tunnel barrier in an HF chemical mixture.

10. The method of claim 3, wherein:

the etching of the anodized tunnel barrier over a second junction mask further comprises wet etching the anodized tunnel barrier with a dilute mixture of HF, nitric acid and deionized water; and

the etching of the anodized portion of the base electrode over the second junction mask further comprises etching the anodized portion of the base electrode in a CHF3 based reactive ion etch subsequent to the etching of the anodized tunnel barrier.

11. The method of claim 2, wherein the etching of the counter electrode layer over a first junction mask further comprises etching away all of the counter electrode layer except for the counter electrode layer within the tunnel junction region.

12. The method of claim 1, wherein the anodizing of the exposed portion of the tunnel barrier layer and sidewall portions of the tunnel junction region further comprises anodizing the sidewall portions of the tunnel junction region to form the junction contact to have a diameter of approximately 1.0 μm or less.

13. A method of fabricating a superconductor integrated circuit from a trilayer comprised of a counter electrode layer, a tunnel barrier layer and a base electrode layer, the method comprising:

anodizing an outer side wall perimeter of a predetermined portion of the counter electrode layer, a predetermined portion of the tunnel barrier layer and a predetermined portion of the base electrode layer for forming an anodization layer; and

etching the anodization layer with at least a first etch chemical mixture for forming an anodization ring from a predetermined portion of the anodization layer, the anodization layer surrounding the predetermined portion of the counter electrode layer, the predetermined portion of the tunnel barrier and the predetermined portion of the base electrode layer.

14. The method of claim 13, wherein the anodizing of an outer side wall perimeter of a predetermined portion of the counter electrode layer is further for forming a junction contact having a diameter of approximately 1.00 μm or less.

15. The method of claim 13, wherein the etching of the anodization layer with at least a first etch chemical mixture further comprises etching the anodization region with the first etch chemical mixture that includes CHF_3, O_2, argon and etching within an etch chamber at a pressure of approximately 25 mTorr and at a power of approximately 300 W.

16. The method of claim 15, wherein the etching of the anodization layer with the first etch chemical mixture that includes CHF_3, O_2, argon and etching within an etch chamber at a pressure of approximately 25 mTorr and at a power of approximately 300 W further comprises subsequently etching with a second etch chemical mixture that includes CHF_3 and O_2 within the etch chamber at a pressure of approximately 100 mTorr and at a power of approximately 150 W.

17. The method of claim 13, further comprising:

etching a portion of the base electrode to form an electrode isolation region for device isolation;

depositing an oxide layer over the base electrode, the electrode isolation region and the anodization ring for forming a dielectric layer; and

etching the dielectric layer for forming a base electrode via and an outside contact via, wherein the anodization ring functions as an etch stop during the etching of the dielectric layer.

18. A superconductor integrated circuit comprising:

a base electrode layer;

a tunnel barrier layer disposed above the base electrode layer;

a counter electrode layer disposed above the tunnel barrier layer; and

an anodization ring disposed around a perimeter of the counter electrode layer and a perimeter of the tunnel barrier layer for preventing a short-circuit between an outside contact and the base electrode layer,

wherein:

a tunnel junction region is defined by the counter electrode layer, the tunnel barrier layer and the base electrode layer, the tunnel junction region including a junction contact defined by a top surface of the counter electrode, the junction contact having a diameter of approximately 1.00 μm or less.

19. The superconductor integrated circuit of claim 18, wherein the base electrode includes an electrode isolation region disposed approximately 0.8 μm or less in horizontal distance from the junction contact for providing device isolation.

20. The superconductor integrated circuit of claim 18, further comprising

a patterned oxide layer disposed above the base electrode layer and the anodization ring for defining an outside contact via and a base electrode via, wherein a surface area of the outside contact via is greater than a surface area of the junction contact.

21. The superconductor integrated circuit of claim 20, further comprising a wire layer disposed above the oxide layer for providing an outside contact and a base electrode contact, wherein a surface area of the outside contact is greater than a surface area of the junction contact.

22. The superconductor integrated circuit of claim 18, wherein the counter electrode layer is disposed solely within the anodization ring.

23. The superconductor integrated circuit of claim 18, wherein the anodization ring is comprised of an anodized portion of the counter electrode layer, an anodized portion of the tunnel barrier layer and an anodized portion of the base electrode layer.

24. The superconductor integrated circuit of claim 18, wherein the tunnel barrier layer is disposed solely within the anodization ring.

25. The superconductor integrated circuit of claim 18, wherein:

the base electrode layer and the counter electrode layer are comprised of niobium;

the tunnel barrier layer is comprised of a layer of aluminum and a layer of Al_2O_3 disposed above the layer of aluminum; and

the anodization ring is comprised of Al_2O_3 and Nb_2O_5.